REMARKS

Applicant has carefully reviewed the Office action from the Examiner dated June 15, 2005 and respectfully request reconsideration. The above amendments and these remarks are submitted in response to the Office Action. Claims 1- 10 and 21-26 are now pending in this case for prosecution. Claims 221-26 have been added. Claims 1,5, 9 and 10 have been amended. Claims 1, 11, 18, 21, and 26 are independent.

Claims 5, 9 and 10 stand rejected under 35 U.S.C. §112, as failing to comply with the written description requirement and as being indefinite. Applicant has amended the claims accordingly, thus rendering the Examiner's rejections moot. Specifically, claims 5, 10 and 9 have been amended to provide antecedent basis and consistency with the specification.

Claims 1-6 and 10 stand rejected under 35 U.S.C. §102 as being anticipated by Frisina. With respects to the Examiner's remarks relating to claims 1-6 and 10, the Examiner contends that the Frisina patent anticipates Applicant's claimed invention. Applicant traverses this rejection and asserts that nothing in Frisina teaches or suggests the amended and newly claimed aspects of the invention provided herein. To the contrary, Frisina is directed to a completely different type of device, i.e. MOS. Frisina teaches that multiple columns of doped regions are required for a high voltage semiconductor device. Further, there is nothing in Frisina that teaches or suggests that there is a variation in the thickness of any particular layer in which the current localization region is formed. Even further, nothing in Frisina teaches or suggests a variation in thickness of layers relative to the central portion of the current localization region.

Frisina is directed to a method of manufacturing an edge structure for a high voltage power MOS device. Frisina attempts to achieve low resistance in its device by stacking a multitude of P-diffused regions. See Abstract " The second step up to the sixth step are repeated at least one time in order to form a final edge structure including a number of superimposed

semiconductor layers of the first conductivity type and **at least two columns** of doped regions of the second ...". Frisina creates an edge structure having a decreasing number or P-diffused regions per stacked layer shifting from the active area of the device the outside. At Col. 3, lines 53-60, Frisina emphasizes the requirement of multiple regions as well as the geometric relation of the various regions. These are features which are specific and restricted to MOSFET manufacturing requirements and concerns.

Applicant's invention is directed to a simple P/N junction diode, in which a single current localization region is created. Applicant's invention also keeps the resistance of the device low while providing a significant lowering of electric fields at the periphery of the device. In an embodiment of Applicant's invention the second layer has a varying thickness, wherein the thickness in the central portion is less than the thickness at the periphery of the device.

Applicant's invention as claimed is not anticipated, nor is it suggested by Frisina as asserted by the Examiner. Frisina does not teach or suggest a semiconductor device having a low electric field at the periphery, with a single current localization region. To the contrary, as clearly set forth above and detailed in Frisina, there is a requirement for multiple P-regions, and such regions have a shape that is inconsistent with the shaped specified by Applicant's invention wherein, "distance in a central portion of the device ... to the third layer of semiconductor material is less than a distance from the first layer of semiconductor material to the third layer semiconductor material at the edge of the device"), See claim 5 of Applicant's specification, see also Figs.2 and 3. Further, Applicant's invention provides a low resistance device with a single localization region. This feature is contrary to the characteristics of Frisian's device, which requires multiple P-diffused regions that are stacked. Even further, the structure of the device disclosed and taught in Frisina is quite distinct from that of Applicant's invention. Frisina

teaches a multi-stacked layered device. Col. 4, lines 18-22. Applicant's amendment of claim 1 further clarifies this distinction.

The Examiner rejected claims 7 and 8 as being unpatentable under 35 U.S.C §103 over Frisina in view of Porter et al. Applicant's remarks respecting claim1 are applicable hereto. Frisina does not disclose all of the limitations of Applicant's claimed invention, as contended by the Examiner. Specifically and as stated above, Frisina discloses a MOS device and as such does not teach or suggest a diode, with a single current localization region. A MOS device cannot possibly have a singe localization region.

Further, Porter is directed to an electrostatic discharge (ESD) protection device. Specifically, Porter is directed to protection for MOS devices. There is nothing to suggest or motivate one skilled in the art to take the teachings related to an ESD for MOS devices, and combine it with the teachings for an edge structure in a MOS device, to arrive at Applicant's invention, which is directed to high voltage p-n junction diodes. As would be understood by one skilled in the art, a diode and a MOS device are quite distinct. There are numerous characteristics and considerations, which are relevant to one device e.g. MOSFET, without necessarily being of any concern in the other device e.g. the p-n junction diode.

In order for the combination of Frisina and Porter to render the claimed invention unpatentable, the references must be combinable and the combination must teach or suggest all the limitations of the claimed invention. It is incumbent upon the Examiner to look to the purpose and use of each of the cited references to determine if the references are properly combinable. A desirability of the combination must be specifically set forth by the Examiner. The resultant combination is not obvious unless the prior art also suggests the desirability of the combination. (See *In Re: Mills, 916 F.2d 680, 16 USPQ 2d 1430 (Fed.Cir.1990.)*. Even if the

cited references are properly combinable they do not teach or suggest Applicant's invention, alone or in combination. The cited prior art deal with a different set of problems that pertain to MOSFET's, as opposed to pn diodes. "Nothing in the references alone or together suggest the claimed invention as a solution to the problem..." *Lindermann Maschinnenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984).*

This aspect is further clarified by the amendment to the parent claim 1. There is nothing within either of the cited references to suggest or motivate one of ordinary skill in the art to make the modification suggested by the Examiner. Applicant believes that the amendments and remarks place the application in condition for allowance or in better form for appeal and thus request their admittance. Applicant further requests the withdrawal of the Examiner's rejection.

If any issue regarding the allowability of any of the pending claims in the present application could be readily resolved, or if other action could be taken to further advance this application such as an Examiner's amendment, or if the Examiner should have any questions regarding the present amendment, it is respectfully requested that the Examiner please telephone Applicant's undersigned attorney in this regard.

Respectfully submitted,

Date: October 14, 2005

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